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**Reg. No. : .....**

**Name : .....**

# Third Semester B.Tech. Degree Examination, April 2015
## (2013 Scheme)
## 13.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer for **all** questions. **Each** question carries **2** Marks.

1. Simplify the expression,
   $Y = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C} + AB\overline{C} + ABC$
2. Write the canonical POS expression for the given function, $f(x,y,z) = \pi M(0,1,5,7)$.
3. Define fan-out and noise margin.
4. Realise a clocked SR Flip Flop with logic gates.
5. Differentiate latch and Flip Flop.
6. Give any two applications of timing circuits.
7. Define flow table for an asynchronous sequential network.
8. How the state diagram helps to realize a logic circuit ?
9. Give the basic structure of a Configurable Logic Block (CLB) ?
10. Give the syntax for array declaration in VHDL. **(10×2=20 Marks)**



PART – B

Answer **any one** question from **each** module. **Each** full question carries **20** Marks.

### Module – I

11. a) Realise the function with the help of a multiplexer,
    $f(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$ **8**

    b) Simplify $P = \pi(0,1,2,3,8,9,11,13,15)$ using K-map and implement the circuit using logic gates. **12**

OR

12. a) Reduce $S = \Sigma 1,3,5,12,14 + d(2,10,15)$ using Quine McCluskey method. 14

b) What is decoder ? Derive logic diagram for 4 to 10 line decoder. 6

## Module – II

13. a) Explain :

i) Excitation table and

ii) State diagram with an example in each case. 8

b) Draw the circuit of master slave flip flop and explain its mode of operation. 12

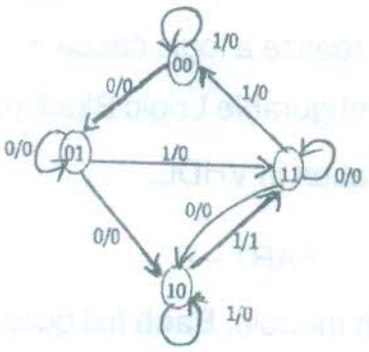
OR

14. a) Design a synchronous counter for generating the given sequence 0,5,1,7,3, the sequence is self starting and repeating, draw the logic diagram also. 10

b) What is a shift register ? How it has classified ? Explain briefly. 10

## Module – III

15. a) Design a sequential circuit of the following state diagram and implement with D Flip Flop. 10




b) Design a suitable state machine for the following conditions, that has an input 'w' and output 'z'. The machine is a sequence detector that produces z=1 when the previous two values of 'w' were 00 or 11, otherwise 'z'=0. Give state table, state diagram, state assigned table. 10

OR

16. a) Reduce the given flow table and find a state assignment table that allows this FSM to be implemented as simple as possible, preserving the Moore model. Derive an excitation table also. 14

| Present State | Next State (w2 w1) | | | | Output z |
|---|---|---|---|---|---|
| | 00 | 01 | 10 | 11 | 0 |
| A | A | E | C | - | 1 |
| B | - | E | H | B | 0 |
| C | G | - | C | F | 1 |
| D | A | D | - | B | 0 |
| E | G | E | - | B | 0 |
| F | - | D | C | F | 0 |
| G | G | E | C | - | 0 |
| H | A | - | H | B | 1 |



b) Give state table reduction methods. 6

## Module – IV

17. a) Discuss the input output characteristic of a TTL gate. 10

b) Write the VHDL code for a JK Flip Flop with behavioral model. 10

OR

18. a) Differentiate PAL and PLA with the help of a neat structural diagram. 10

b) Construct a combinational circuit with ROM for accepting three bit numbers and generates an output number equal to the square of the input number. 10